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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: David H. EPPES et al.

Docket: AMDA.477PA

Title: INTEGRATED CIRCUIT RESISTIVE HEATING SYSTEM AND METHOD THEREFOR

CERTIFICATE UNDER 37 CFR 1.10
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- ☒ Transmittal sheet containing Certificate under 37 CFR 1.10.
- ☒ Patent Application: Pages Numbered 1-20 ; 30 claims; Abstract 1 pgs.
- ☒ 2 sheets of formal drawings
- ☒ An unexecuted Declaration
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AMDA.477PA (TT4018)
June 2, 2000

INTEGRATED CIRCUIT HEATING SYSTEM AND METHOD THEREFOR

Related Patent Documents

This application is related to and fully incorporates U.S. Patent Application Serial No. _____ (AMDA.478PA), entitled "Internal Heating System and Method Therefor," and filed concurrently herewith.

Field of the Invention

The present invention relates generally to semiconductor analysis and, more particularly, to semiconductor analysis involving temperature control of a semiconductor die.

Background of the Invention

The electronics industry continues to rely upon advances in semiconductor technology, including integrated circuits (ICs), to realize higher-functioning devices in more compact areas. For many applications, realizing higher-functioning devices requires integrating a large number of electronic devices into a single silicon die. In addition, many of the individual devices within the die are being manufactured with smaller physical dimensions. As the number of electronic devices per given area of the silicon die increases, and as the size of the individual devices decreases, testing processes become more important and more difficult.

Many integrated circuit dice include circuits having random defects. These defects can recover or fail under particular operating conditions and at higher

temperatures. In addition, design faults can be sensitive to such particular operating conditions. Traditionally, isolation of IC faults has been attempted by operating the die in a manner that causes a failure to occur and by attempting to attribute the failure to a malfunctioning circuit element in the IC. One manner in which this has been performed is to operate the die at full speed while applying external heat to the die. Such electrical testing, however, does not always assist in fault isolation because many failure symptoms can manifest themselves in different ways, and malfunctions can result from a variety of different types of defects including defects at non-suspect circuitry locations.

One such testing application that has traditionally been very difficult to accomplish includes physical diagnosis of failing circuit paths in a semiconductor die. Identifying these "critical circuit paths" has been attempted using simulation in conjunction with a thorough understanding of semiconductor die design, followed by verification using physical probing of a suspect circuit. This physical analysis is difficult, however, because it generally requires intimate knowledge of the die design and is particularly difficult for use in analyzing a flip-chip type integrated circuit die. The identification and analysis of critical circuit paths continues to present a challenge to the advancement of the semiconductor industry.

Summary of the Invention

The present invention is directed to a method and system for analyzing a semiconductor die involving the selective application of heat to the die. The present

invention is exemplified in a number of implementations and applications, some of which are summarized below.

According to an example embodiment, the present invention is directed to a method for analyzing a semiconductor die using a particular application of heat. A region-selective heater having a plurality of heating elements is thermally coupled to the semiconductor die. Various ones of the heating elements are selectively caused to generate heat while the die is operating. The generated heat is used to heat a portion of the die, and a response, such as a failed operation, is detected in connection with analysis of the die. This enhances the ability to identify defects as well as critical circuit paths including, for example, critical timing circuit paths of the semiconductor die; and can be performed without necessarily using expensive laboratory test equipment. In addition, this method does not necessarily require operating the die at a known failing condition or under precisely controlled ambient temperature and voltage conditions.

According to another example embodiment of the present invention, a system is adapted to selectively heat a semiconductor die and to analyze the die in response to the selective heating. The system includes a region-selective heater having a plurality of heating elements and a coupler adapted to couple the heating chip to the die in a manner that makes possible heat transfer from the chip to selected regions of the die. A controller is adapted to activate the heating elements to present heat to selected portions of the die therefrom. The die is operated using a testing device coupled to the die, and a detector is adapted to detect a response from the die.

The above summary of the present invention is not intended to describe each illustrated embodiment or every implementation of the present invention. The figures and detailed description that follow more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 shows a region-selective die heating system, according to an example embodiment of the present invention; and

FIG. 2 shows an example grid arrangement for use in a region-selective die heating system, according to another example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not necessarily to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description

The present invention is believed to be applicable for a variety of different types of semiconductor devices, and the invention has been found to be particularly suited for an integrated circuit dice requiring or benefiting from analysis involving the selective

application of heat to the die in order to locally heat a portion of circuitry in the die. While the present invention is not necessarily so limited, aspects of the invention may be appreciated through a discussion of various examples using this context.

According to an example embodiment of the present invention, a heating arrangement is adapted to selectively heat one or more portions of a semiconductor die, such as a wire-bond or flip-chip type die. The heating arrangement includes a region-selective heater that includes a plurality of heating elements. The region-selective heater can be implemented in various arrangements to facilitate selected testing of the die, such as to provide access to the die through the heater, or to couple only to a portion of the die. In one implementation, the heater is provided in a "chip." Other implementations include providing the heater in an adhesive strip, in a semiconductor package substrate, or in any suitable package adaptable to thermally couple to a semiconductor die.

In this particular example embodiment, the region-selective heater is coupled to the die using a common fastener or suitable adhesive. In the case of a flip-chip type die, the heater is coupled to the die over the back side. In the case of a wire-bond die, the heater is placed on a die package, and the die is placed over the heater and bonded to the package via wire-bonds. In one particular implementation, the heater is electrically coupled to the package and operated with an electrical signal provided to the heater via the package. In another particular implementation, the heater is formed in a package to which a wire-bonded die is attached.

Once the heater is coupled to the die, it is connected to an integrated circuit tester and operated to heat selected locations of the die in response to a control input.

The tester applies a test pattern to the die and the die is monitored for any defective operation that would indicate a die malfunction. When defective operation is detected, the corresponding portion of the die being heated is identified as a portion having a suspected defect. Once a portion of the die containing a defect is identified, the die is probed to provide additional defect information.

Various types of defects, such as resistive vias, timing-related defects, defective transistors, short or open circuits and other circuit defects are detectable using the heating arrangement. In the case of detecting timing defects, circuit paths in the die that fail upon operation at high speed or under heat application are often known in view of the design layout. These critical timing paths tend to fail before other portions of the die. The selective addition of heat to the die is used to cause a selected critical timing path to heat, and the increased heat makes the critical timing path more susceptible to failure. When a failure occurs while a particular critical timing path is heated, that failure is an indication that the heated path contains a defect or an improperly designed component of the circuit that fails at higher temperatures. Further analysis is then performed on circuit elements in the critical timing path to better identify the cause of the malfunction.

The integrated circuit tester is adapted to provide multiple test patterns to the die. The test patterns are selected to cause the die to operate in a manner useful for testing purposes. For example, the die can be operated with a normal operation pattern, a preset test pattern, under a high-stress operating condition, or under a test pattern that selectively causes regions of the die to operate. Selectively operating regions of the die is particularly useful for isolating the critical timing paths discussed hereinabove. Input

signals to the die cause circuit elements in a selected critical timing path to operate. Heat is applied to the circuit elements and any defective response is detected and used to identify that one of the circuit elements is suspected of being defective.

In another example embodiment of the present invention, the region-selective heater includes a series of heating elements that are formed in a heating grid. The elements may include, for example, one or more of the following: a transistor, diode, resistive metal trace, polysilicon trace, and a doped substrate area. Such a heating element may include a circuit arrangement having a plurality of semiconductor devices. Each element is coupled to a power supply via interconnects in the heater. When selectively powered, each element generates heat that is used to heat a corresponding portion of the semiconductor die to which the heater is coupled.

In a more particular example embodiment of the present invention, the back side of die is thinned prior to the heater being placed on the back side. Enough substrate is removed from the die to facilitate sufficient heat transfer from the heater to the die. The substrate removal is accomplished using one or more of many removal devices available, employing processes such as CMP, laser etching, FIB and other common processes.

FIG. 1 is a heating system adapted to analyze a semiconductor die, according to another example embodiment of the present invention. A semiconductor die 130 is positioned on a stage 135 and is coupled via the stage to a testing device 140 adapted to generate test signals for the die. Commonly-available testing devices, such as the Teradyne J971, are suitable for stimulating the die. A heater 110 is coupled to the die, and the heater includes a plurality of heater elements adapted to generate heat in

response to being powered. In one implementation, the heater is fastened to the die using a fastener, such as a clamp or other mechanical device, or an adhesive used to fasten the heater to the die. A controller 120 is communicatively coupled to the heater 110 and provides a control signal that causes one or more selected heating elements to operate. The die is operated via the testing device, and a response to the combined heat and operation is detected. The response may, for example, be detected using the testing device itself, or other common laboratory detection devices (*e.g.*, analytical equipment such as an electron beam or laser beam probing system) may be implemented in replacement thereof or in addition thereto. The detected response is then used to analyze the die. Optionally, a computer device 150 is coupled to the controller 120 and/or the testing device 150, and is used to communicate control, response or other data. Response data is provided via the computer for user review.

Once a malfunction of the die has been detected, the portion of the die that is defective or otherwise limited by a design flaw is identified. One example manner in which to identify a defect is to obtain an image of the defective portion of the die, such as a cross-sectional image, and examine the image to identify a particular circuit element that is defective. Another manner is to correlate the location of the heater element causing the defect with a known circuit layout and identify the defective portion of the die therefrom. In another implementation, the computer arrangement is adapted to use the detected response to perform the die analysis, such as by storing or manipulating the response, or by displaying information depicting the particular heater element being operated in order to isolate a critical timing path. The stored or displayed

information can then be compared to empirical data, such as for a properly-functioning die, and variances in the comparison indicate a malfunction.

FIG. 2 shows an example grid arrangement of heater elements, according to another example embodiment of the present invention. The grid may, for example, be implemented in connection with heater 110 of FIG. 1. Each intersection of the grid has a heating element. The elements are referred to by their row (capital letters) and column (numbers) identifications. For example, the element A1 at the circled intersection is identified as such because it is in row A, column 1. The grid elements may include various heat-generating circuitry, such as those elements mentioned hereinabove. In addition, the heater elements can be operated individually, together, in patterns or in virtually any manner consistent with the various applications of the present invention.

In another example embodiment of the present invention, a feedback loop is coupled to one or more of the heating elements. The feedback loop is used to control the action of the heating element. As the temperature changes, the loop is used to provide an indication of the change. This indication is used to detect various aspects of the heat application, such as the temperature, a change in the temperature and a rate of change (increase or decrease) in the temperature. Using the indication supplied by the feedback, the heat application is optimized to meet a desired response. Optimization includes maintaining parameters such as a selected temperature, a selected rate of increase or reduction of heat application and a selected heat differential from one area to another. In addition, the feedback can be used to detect the amount of heat spreading to

surrounding circuitry, and the accuracy of the heat application can be detected therefrom.

In one implementation, the heating element is a transistor having a gate and controlled by way of an electrical bias provided to the gate. In this instance, the feedback loop includes a temperature sensor, such as a temperature sensitive diode, temperature sensitive transistor or a thermocouple. The temperature sensor is coupled to the gate and, as the temperature changes, the sensor applies a bias to the gate that is related to the temperature change. This bias in turn affects the amount of current flowing through the transistor, and thereby regulates the amount of heat generated by the operation of the transistor. For instance, as the temperature increases, the bias applied to the gate via the sensor causes the amount of current flowing through the transistor to decrease, and less heat is generated. Similarly, as the temperature decreases, the bias applied to the gate causes the amount of current flowing through the transistor to increase, and more heat is generated.

In another example embodiment, temperature feedback is used to control the region-selective heater. When the temperature exceeds a selected level, the heater is caused to generate less heat. This is accomplished in different manners, depending upon the application. In one implementation, the heater is operated at a selected operating speed. When the temperature feedback indicates that the amount of heat being supplied is too much, the operating speed is slowed. If more heat is needed, the operating speed is increased. The amount of power supplied to the heater can be altered to control the heat generation in a similar manner.

Monitoring the temperature can be implemented in various ways. In one embodiment, the voltage across an active (transistor) arrangement in a target or representative region in the die is measured at output ports of the heating chip wherein a change in the voltage correlated change in temperature in the target region of the heating chip and/or the die. Depending on the sophistication of the heating chip, the temperature correlation is implemented separate from the die / heating-chip arrangement, *e.g.,* manually or using a computer or calculator, or is implemented using logic and translation devices (such as an analog-to-digital converter for converting the sensed voltage differential to a readable digital temperature code) internal to the heating-chip. Alternatively, the logic and translation devices can be piggy-backed onto the heating-chip and electrically connected to the output ports of the heating chip.

The region-selective heater may be operated in various fashions. In one example embodiment, a control register is formed in the heater, and the control input is effected with the control register. The control register is adapted to selectively activate an individual heating element (such as an arrangement of activatable semiconductor devices) in the heater. The selected element is used to generate heat and thereby heat nearby circuitry in the die. In another example embodiment, the heater is adapted to receive signals from an external control. The external control is used to selectively activate one or more individual heating elements in the heater, and is accomplished either using the control element or by directly activating the heating element. In one implementation, the control input includes a serial signal. Decoding and lookup blocks in the heater interpret the signal and activate one or more heating elements based on the interpreted signal. In another implementation, the external control includes an

activation grid that is electrically coupled to various heater elements in the heater. Selected portions of the grid are activated and corresponding elements in the heater are powered, thereby generating heat. In still another implementation, the activation of the heater elements is pulsed and generates pulses of heat.

The grid operation characteristics are tailored differently to optimize particular testing applications. Various temperature selections and gradients can be used to effect selected tests. In one implementation, the control input is selected to operate various portions of the heater in a sequence. For example, one element can be activated while the remaining elements are left inactive. This provides the ability to selectively heat a small portion of the die being analyzed. In another application, the elements of the heater are heated in a selected sequence. Response data from the die is obtained and recorded relative to the sequence in which the heat is applied.

In another application, heat is applied to a group of elements at a time. A group consisting of adjacent heating elements is selected when it is desired to apply more heat than a single element can provide. This is particularly useful in combination with a feedback loop when a selected temperature is to be maintained. For example, referring to FIG. 2 and using the identification scheme discussed hereinabove, heating elements at locations B1-B4 and C1-C4 are powered, and the die to which the heater is attached begins to heat. If the heating rate is to be increased, additional heating elements at locations A1-A4 and D1-D4 are powered. If the heating rate is to be decreased, heating elements at locations B1-B2 and C1-C2 are shut off. In this manner, the amount of localized heating is readily controlled. Various other combinations are readily available based upon the desired results.

In still another application, and referring again to FIG. 2, the even-numbered elements at locations in rows A, C and E are selectively heated. Selecting elements that are distanced as such caused localized heating in various portions of the die at once, and the distance between the heated elements can be maintained such that heat from each element does not interfere with heat from another element. This is particularly useful, for example, for analyzing groups of critical paths to more efficiently identify defects and to speed the analysis process. If the entire group of critical paths withstand the application of heat via the grid, the heated elements are turned off, another group of elements is powered (*e.g.*, the odd-numbered elements at locations in rows B, D and F), and the test is repeated. Once a defect has been found to exist corresponding to a critical timing path heated by the group of elements, further analysis is performed on portion of the die heated by the group of elements causing a defect.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.

What is claimed is:

1. A method for analyzing a semiconductor die, the method comprising:

thermally coupling a heater having a plurality of heating elements therein to a semiconductor die;

while operating the die, selectively controlling the heating elements and therein causing at least one of the heating elements to heat at least one adjacent portion of the die; and

analyzing the die via the operation and heating.

2. The method of claim 1, wherein operating the die includes running a test pattern on the die suspected to cause a failure.

3. The method of claim 1, wherein operating the die includes electrically coupling the die to a signal generator adapted to supply test signals to the die.

4. The method of claim 1, further including detecting that the die is malfunctioning.

5. The method of claim 4, further comprising:

identifying the portion of the die being heated at the time that a malfunction is detected; and

correlating the portion of the die being heated to a critical timing path.

6. The method of claim 5, further comprising probing circuitry in the critical timing path and determining therefrom the nature of a defect.

7. The method of claim 1, wherein the die includes at least one of: a flip-chip bonded die and a wire-bonded die.

8. The method of claim 7, wherein the die is a wire-bonded die, and wherein coupling the heater to the die comprises:

placing the heater on a die package;

placing the semiconductor die on the heater; and

wire-bonding the semiconductor die to the package.

9. The method of claim 8, further comprising electrically coupling the heater to the package, wherein selectively controlling the heating elements includes applying an electrical signal to the heater via the electrical coupling to the package.

10. The method of claim 1, wherein selectively controlling the heating elements includes causing the die to heat to a selected temperature.

11. The method of claim 1, wherein selectively controlling the heating elements includes heating a plurality of the heating elements in a selected sequence.

12. The method of claim 1, wherein selectively controlling the heating elements includes causing at least two of the heating elements to generate heat, and wherein the at least two of the heating elements are located sufficiently distant from each other so that heat from one of the elements does not interfere with heat from another one of the elements in heating the die.

13. The method of claim 1, wherein selectively controlling the heating elements includes causing the at least one heating element to generate pulses of heat.

14. The method of claim 1, wherein selectively controlling the heating elements comprises:

grouping the heating elements into selected groups, each group having two or more heating elements;

causing the selected groups to heat in a sequence;

detecting a response from the die that indicates that the die is operating defectively; and

in response to detecting the defective operation, identifying the selected group being caused to heat when the response is detected; and

selectively operating individual heating elements of the selected group.

15. The method of claim 1, wherein selectively controlling the heating elements comprises:

detecting a temperature characteristic related to the heat being generated; and

in response to the detected temperature characteristic, controlling the heating via a feedback loop.

16. The method of claim 15, wherein detecting a characteristic of the heat being generated includes detecting a temperature using a temperature sensor located in the heater.

17. The method of claim 1, wherein analyzing the die includes detecting a response from the die, further comprising storing the detected response in a computer arrangement and using the stored response for analyzing the die.

18. The method of claim 1, wherein the die is a flip-chip die, further comprising, prior to thermally coupling the heater to the die, thinning a back side of the flip-chip die, and wherein thermally coupling the heater to the die includes coupling via the thinned back side of the die.

19. A system for analyzing a semiconductor die, the system comprising:

a plurality of heating means, arranged adjacent the die, for heating selected portions of the die;

control means for selectively controlling the heating means and therein causing at least one of the heating means to heat at least one adjacent portion of the die;

operating means for operating the die; and

detection means for detecting a response from the die.

20. A system for analyzing a semiconductor die, the system comprising:

a heating chip having a plurality of heating elements arranged adjacent the die and adapted to heat selected portions of the die;

a controller adapted to selectively control the heating elements and therein cause at least one of the heating elements to heat at least one adjacent portion of the die;

a testing device adapted to operate the die; and

a detector adapted to detect a response from the die.

21. The system of claim 20, wherein each heating element includes at least one of: resistive metal, a transistor, a diode, doped metal and a polysilicon trace.

22. The system of claim 20, wherein one of the heater elements includes a transistor having a gate, and wherein the heater further comprises a temperature sensor coupled to the base of the transistor and adapted to provide feedback to bias the gate, and therein regulate the current through the transistor and control the heat generated.

23. The system of claim 22, wherein the temperature sensor includes at least one of: a diode and a transistor.

24. The system of claim 20, further comprising a stage to hold the die and electrically couple the die to the testing device.

25. The system of claim 20, further comprising a computer communicatively coupled to the tester and adapted to control the tester.

26. The system of claim 25, wherein the computer is further communicatively coupled to the controller and adapted to direct the controller's operation.

27. The system of claim 20, wherein the detector and the testing device are included in a single arrangement.

28. The system of claim 27, further comprising a computer communicatively coupled to the controller, the testing device, and the detector, and wherein the computer is adapted to control the analysis of the die and to provide response results from analysis for review by a user.

29. The system of claim 20, wherein the heater chip further comprises a control register adapted to provide control signals to the heating elements.

30. A method for analyzing a semiconductor die, the method comprising using a plurality of heating elements to selectively heat regions of an operating die and analyzing the die therefrom.

Abstract

Semiconductor die analysis is enhanced via a method and system that use a heater having a plurality of heating elements to heat a selected portion of the die. According to an example embodiment of the present invention, the heater is thermally coupled to the die, and the die is operated while at least one of the plurality of heating elements heats a portion of the die. A response is detected and used to analyze the die. The present invention makes possible selective heating of the die in a manner that is readily controllable and implemented. Die analysis, including, for example, critical timing path analysis, is enhanced by this ability to controllably heat the die.

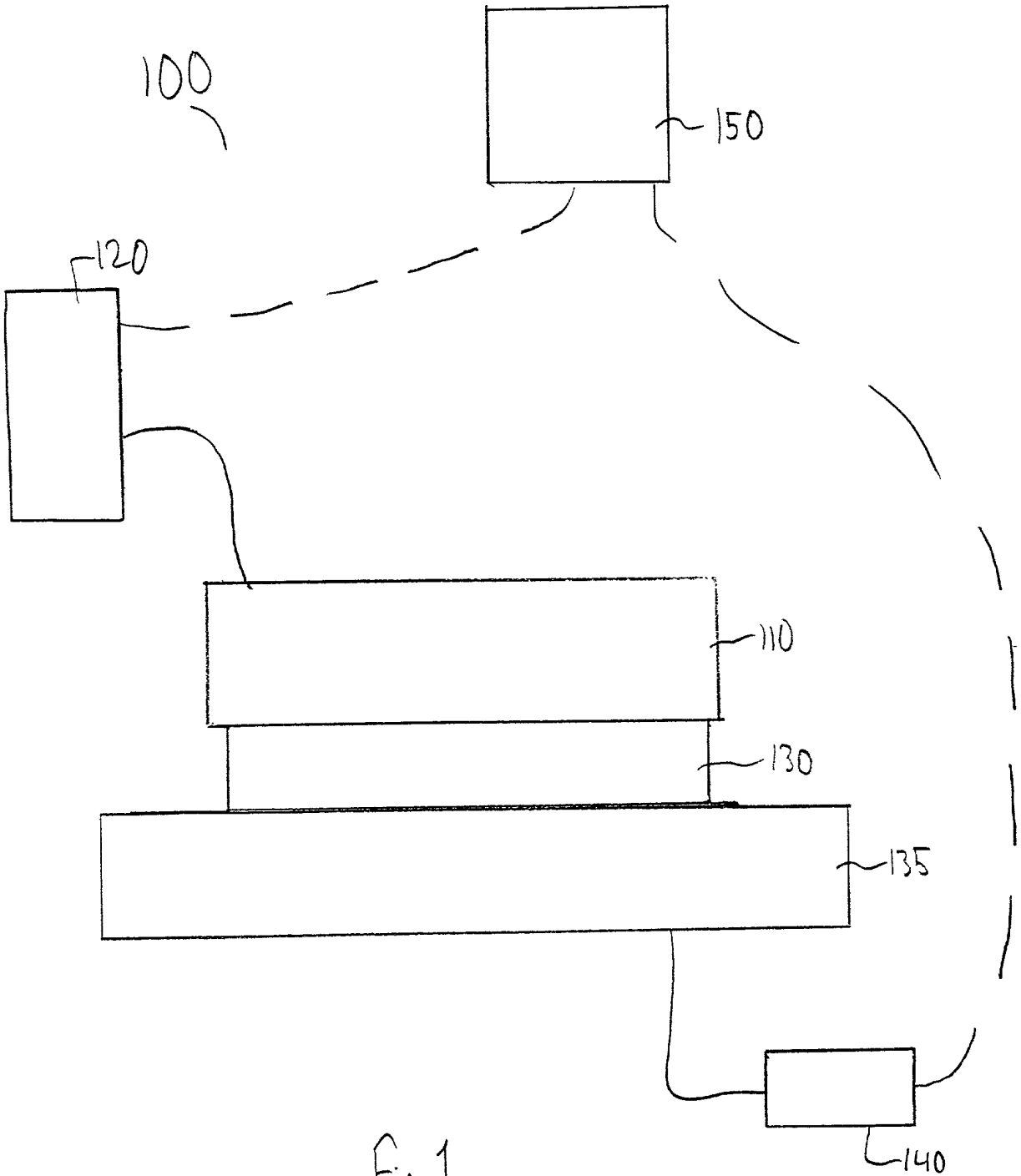

Fig. 1

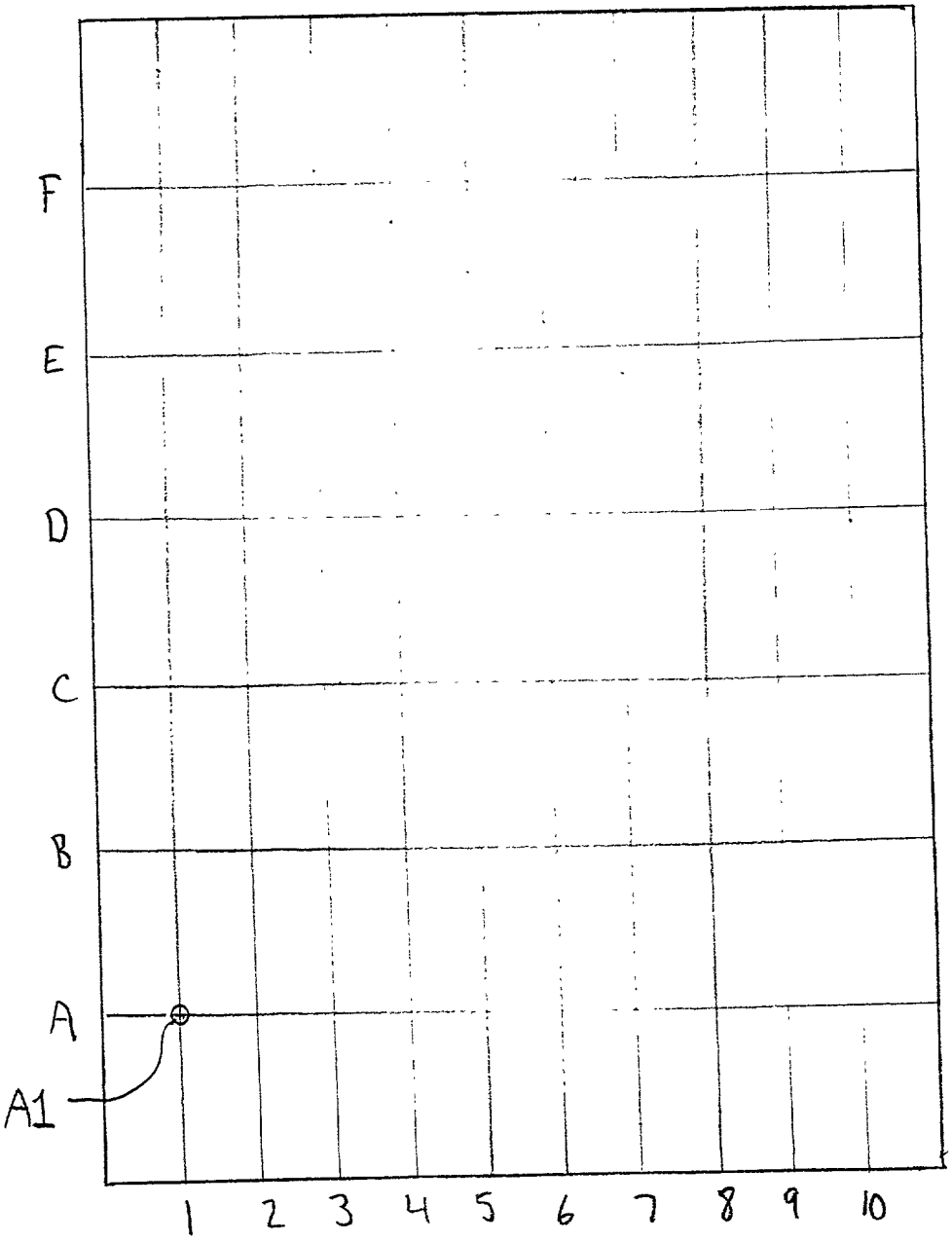

Fig. 2

CRAWFORD PLLC

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **INTEGRATED CIRCUIT RESISTIVE HEATING SYSTEM AND METHOD THEREFOR.**

The specification of which
a. ☒ is attached hereto
b. ☒ is entitled **INTEGRATED CIRCUIT RESISTIVE HEATING SYSTEM AND METHOD THEREFOR,** having attorney docket number **AMDA.477PA (TT4018).**
c. ☐ was filed on as application serial no. and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. filed and as amended on (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications have been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	**APPLICATION NUMBER**	**DATE OF FILING (day, month, year)**	**DATE OF ISSUE (day, month, year)**
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	**APPLICATION NUMBER**	**DATE OF FILING (day, month, year)**	**DATE OF ISSUE (day, month, year)**

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Crawford, Robert J.	Reg. No. 32,122	Jimenez, José W.	Reg. No. 31,113
Maunu, LeRoy D.	Reg. No. 35,274		
Drake, Paul S.	Reg. No. 33,491	Pitruzzella, Vincenzo D.	Reg. No. 28,656
Apperley, Elizabeth A.	Reg. No. 36,428	Roddy, Richard J.	Reg. No. 27,688
Riley, Louis A.	Reg. No. 39,817	Zahrt II, William D.	Reg. No. 26,070

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Crawford PLLC.

Please direct all correspondence in this case to Crawford PLLC at the address indicated below:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	**Full Name Of Inventor**	**Family Name** EPPES	**First Given Name** DAVID	**Second Given Name**
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Signature of Inventor 201:			**Date:**	

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2	**Full Name Of Inventor**	**Family Name**	**First Given Name**	**Second Given Name**
0	**Residence & Citizenship**	**City**	**State or Foreign Country**	**Country of Citizenship**
3	**Post Office Address**	**Post Office Address**	**City**	**State & Zip Code/Country**
Signature of Inventor 203:			**Date:**	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.